Proposal of a New Ultra Low Leakage 10T Sub threshold SRAM Bitcell

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Abstract—**The tendency for low energy consumption in systems-on-chip results in a need for memories operating in the near- and sub-threshold regions. This paper gives a comparative study of Static Random Access Memory (SRAM) bitcells working under Ultra-Low Voltage in 32nm CMOS. A new 10T SRAM bitcell is then proposed and features low leakage current. It is capable of operation under ULV (~300mV) and allows bit-interleaving technique that is critical to cope with multiple bit soft-errors for reducing dynamic and static power consumption compared to state-of-the-art bitcells.**

Keywords:Sub threshold Design, SRAM, Leakage, half selected bitcells, Bitcell.

I. INTRODUCTION

Static Random Access Memory (SRAM) in a System-on-Chip (SoC) contains 50% to 90% of the total chip transistor count in average. It is thus one of the significant sources of energy consumption in SoC operation. In SRAM memory, the total energy dissipation includes static and dynamic contributions:

$$E_{tot} = E_{static} + E_{dynamic} = I_{Leak}.V_{DD}.t_{delay} + \frac{1}{2}.\alpha.C_S.V_{DD}^2 \qquad (1)$$

Where the static energy contribution depends on the total circuit leakage, I_{leak}, and on the delay time, t_{delay}, the dynamic energy contribution depends on the switching capacitance, C_s, and on the activity factor, α, while both energy contributions depend on the supply voltage V_{DD}. One of the most effective ways to reduce the power consumption is to lower V_{DD} as this significantly decreases dynamic power dissipation and static leakage power [1]. However, reducing V_{DD} has a negative impact on the maximum achievable operating frequency and thus on tdelay, and therefore increases the static energy. There is an optimum voltage, V_{Opt}, which allows reaching a minimum energy per operation, which lies near the MOS devices threshold region. In this operating region, and given the large number of bitcells in a SRAM, it is essential to design a bitcell giving the lowest possible leakage current.

Recent research on Ultra-Low Voltage SRAM memories has shown that V_{Opt} is in the range between 300 mV to 500 mV [2]. Achieving successful low-voltage operations in SRAM faces a considerable amount of challenges due to the reduced bitcell stability and the degraded Ion-to-Ioff ratio, and the reduced voltage margins due to the increase in device variability. Random Dopant Fluctuations (RDF) [3] causes large threshold voltage variability that impacts directly the SNM (Static Noise Margin, [4]) and WM (Write Margin, [5]) of the bitcell. Furthermore the sensing and the overall architecture are difficult to design due also to the CAD device model being less precise in the sub-threshold region [6].

This paper reviews some major bitcells available in literature and proposes a new 10T bitcell to reduce the leakage current. It is also demonstrated that the parasitic dynamic power consumption is reduced with the proposed bitcell. The paper is organized as follows: Next Section covers the state-of-the-art on Ultra-Low Voltage (ULV) bitcells. The proposed SRAM bitcell is detailed in Section III. The overall bitcell simulated performances are compared in Section IV. The simulation results confirm the interest of this new 10T bitcell that is being processed in 28nm CMOS technology.

II. CONSTRAINTS AND LIMITATIONS OF AVAILABLE BITCELLS

A conventional six–transistor (6T) SRAM bitcell is based on the use of a latch built with two cross-coupled CMOS inverters, the contents of which can be accessed through two nMOS access transistors. However, operating a conventional 6T at Low Voltage (LV) with a good yield is challenging, since the bitcell read-stability and its write-ability get degraded and cannot be both optimized at the same time at a given area, since they have conflicting design requirements. This section reviews the most common limitations of SRAM bitcells in ULV operations.

A. Soft Error (SE) disturb

In memory circuits or sequential logic, a SE is caused by an energetic particle that enters the chip and generates enough free charges to toggle the state of a latch [7]. The sensitivity to SEs is directly related to the cell capacitance: the smaller the capacitance, the greater the sensitivity [8].
At each new technology node, due to the surface shrink and its related capacitance shrink, the bitcells become more sensitive to SEs. Since the sensitivity increases as the voltage is scaled down [9], SEs are more critical for sub-threshold SRAMs than for standard voltage SRAMs and require to use a so-called bit-interleaving technique in the memory architecture [10].

B. Bit-Line Leakage

In high-speed operations, it is common to use a sense amplifier when a bitcell is accessed, to detect differentially the

droop on one of the read bit-lines with respect to the other, in order to quickly detect the data cell content. However, both bit lines are discharged also by the leakage current of all access transistors tied to it. The differential readout works if the read-current of the accessed-cell is able to discharge a bit-line more quickly than the aggregate leakage-current of all other N_r bitcells tied to the other bit-line in the same column.

Reducing V_{DD} degrades the so-called Ion-to-Ioff ratio, which is equal to $I_{Cell}/ (N_r*I_{Leak, BL})$, and sets an upper limit to the number of bitcells Nr that can be stacked in a column.

C. *Effects of temperature and doping on Mobility*

In a semiconductor, both mobility and charge carrier concentration are temperature dependent. It is thus important to view the conductivity as a function of temperature and concentrations.

Fig. 1 and Fig. 2 show the histograms of the read current, Iread, of the bitcell in [10] that will be described later, at three different temperatures (-40°, 27° and 125°), as obtained with Monte Carlo (MC) scheme on SPICE simulations at ULV (Fig. 1) and at 1 V (Fig. 2).

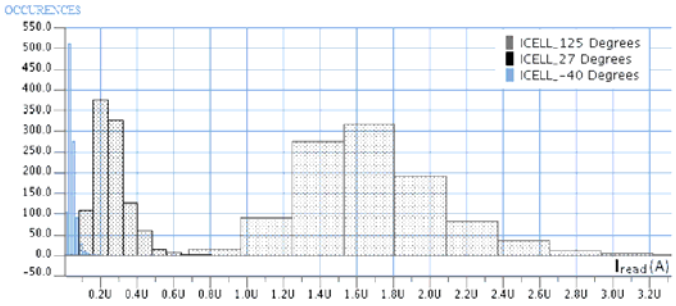

Figure 1. Monte-Carlo simulation of I_{read} (1024 runs), V_{DD}=300 mV (Corner Process TT)

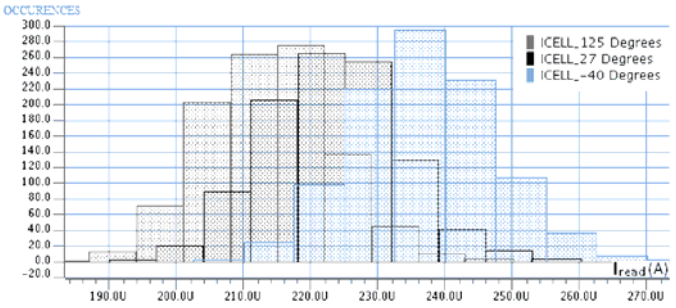

Figure 2. Monte-Carlo simulation of I_{read} (1024 runs), V_{DD}=1V (Corner Process TT)

The peak of the distribution in Fig. 2 gives the most probable I_{read} value. It is noticeable that the current value is smaller with higher temperature. This phenomenon is related to the channel mobility degradation with temperature. This tendency is reversed at ULV (Fig. 1). The carrier-pair thermal generation counterbalances the mobility degradation at ULV. The spread of the distributions is reduced at ULV while it is rather constant at 1V. Fig. 1 gives evidence of a low I_{read} current value at UVL at low temperature.

D. *Dynamic energy losses*

As already stated, the bit interleaving technique can resolve multiple bit soft-errors at ULV. Figure 3 shows an implementation using two pass-gate transistors in the bitcell [10]. When a bitcell is selected either for read or write operation, all bitcells located in the same Write Word-Line (WWL) are half-selected and have floating potential on their bit lines. The words that are not selected suffer during read and write operations from additional power losses, which are due to discharge of these unselected bit lines. The parasitic components behavior in unselected bitcells in selected line directly affects the dynamic energy consumption as it is the case in the standard 8T bitcell and the 10T bitcell in [10].

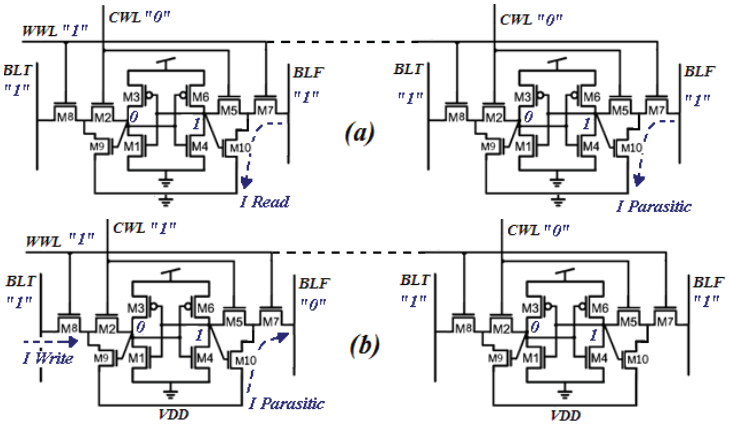

Figure 3. Behavior of the 10T bitcell in [10] (a) Read (b) Write operations

During write operation a parasitic current is also injected from V_{DD} to BLF as in Fig 3 (b). To avoid this phenomenon, the easiest way is to use one word per line. There is no more unselected bitcells in the selected line. Unfortunately this technique increases the number of lines with negative impact on the complexity of the SRAM memory architecture. Moreover the number of lines is limited and finally the gain in the latter dynamic power losses is very small: it is not worth the limitations.

We propose here the implementation of a multiplexing technique to allow multiple words per line but with limited effects of the non selected bitcells.

III. PROPOSED 10T BITCELL

Fig. 4 (a) shows the schematic of the proposed 10T SRAM bitcell. This symmetrical cell comprises two cross-coupled CMOS inverters and two pass-gate transistors in series to allow the use of a bit-interleaving technique. This guarantees a highly resistive path between bit lines and internal data nodes. A virtual read word line (RWL_MUX) is introduced to read the bitcell through two decoupled transistors (M9, M10). The read transistors are used to transfer the data to the read bit lines (RBLT, RBLF). Figure 4 (b) shows the layout of the proposed bitcell as implemented in 28nm bulk CMOS manufactured by STMicroelectronics with 0.8 μm^2 areas. The transistors in the read path have been sized in order to have an acceptable value for SNM and read current under worst case conditions at 300

mV. In order to have a proper functionality during the write operation (to avoid parasitic current between the RWL_MUX and bit line), the proposed bitcell requires the use of four bit lines. The 4 bit lines design comes with no silicon penalty at bitcell level but introduces a minimal routing constraint within the memory cut.

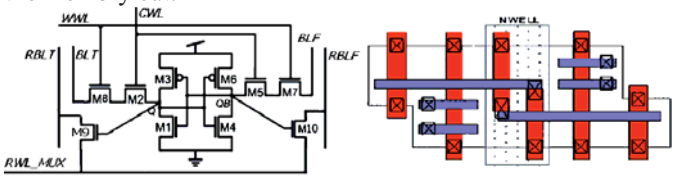

Figure 4. Proposed 10T ULV Bitcell. (a) schematic (b) Layout.

A. A hard coding technique:

Fig 5 shows a proposed hard coding technique in order to solve the half-select cell bit lines issue. The idea of this technique is to multiplex the RWL_MUX signal according to the number of words per line. This allows selecting only one word during the reading operation and hence eliminates the issue of the parasitic dynamic energy losses from the unselected bit lines.

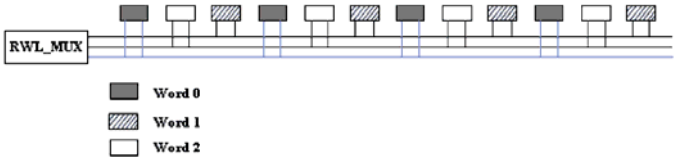

Figure 5. Proposed hard coding technique

The RWL_MUX signal is at the source of the two read access NMOS transistors (M9, M10).

In the read operation, RWL_MUX=V_{SS}: only for the selected word. For the other bitcells, it is selected to V_{DD}.

In the write and standby operations, RWL_MUX=V_{DD} for all cells.

B. A new solution for the charge injection issue:

Fig. 6 shows that during the read operation, there is a struggle between the read current, I_{read}, taken from the selected bitcell and the injected current, $I_{Injected}$, from the non-selected bitcells, from RWL into RBL. So, solving the latter issue requires that the sense amplifier reacts before RBL bit line reaches V_{SS}. During the read operation, a small voltage difference ΔV between the RBLT and RBLF will then be developed and must be sensed by the differential sense amplifier.

The sense amplifier must react quickly in order to have a differential voltage ΔV that remains below the threshold voltage. For other bitcells of the column, the gate-source voltage of the transistors M9 and M10 is at most equal to ΔV. These transistors are therefore blocked. In addition, the drain-source voltage of transistors M9 and M10 for unselected bitcells of the column is not greater than ΔV so that leakage currents are low.

However, designing a fast sense amplifier operating at ULV is a challenging task due to the global and local variations. Also this solution requires introducing of an additional negative power supply.

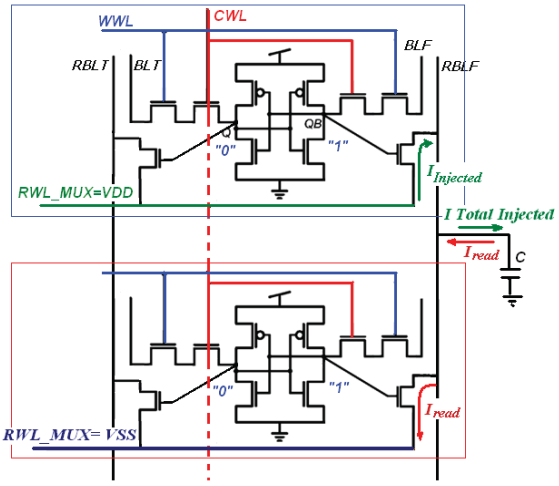

Figure 6. The charge injection issue

As a solution to this problem, it is proposed to introduce a transmission gate at the RWL, which will stop the current injected from RWL into the RBLs in the unselected bitcells from the selected column and therefore eliminate the charge injection issue (Fig. 7).

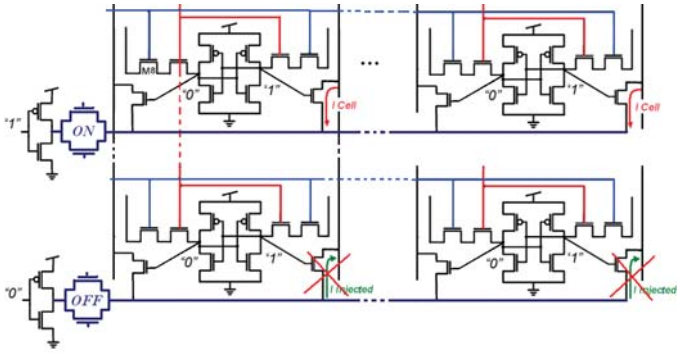

Figure 7. Proposed solution to avoid the charge injection issue

C. A novel technique to increase the number of bitcells per column

During the read access, the cell read current of a single cell discharges the RBL (Read Bit line). If N cells are connected to the RBL pair, the worst-case data pattern is when N-1 cells discharge the complementary RBL with their leakage currents. When N is large and the I_{on}/I_{off} ratio is small, the discharge of the complementary RBL can be of the same magnitude as the discharge of the active RBL. This can result in an incorrect sensing of the data. This problem is due to the decrease in the read current under ULV. Hence there is a limitation of the number of bitcells per column. For a correct assessment, the variations of Ion and I_{off} must be taken into account.

The multiplexing technique in Fig. 8 is designed for bitcells with 4 bit lines. The idea is to multiplex several bit lines for reading and keep the write bit lines common for all bitcells in the column. This technique allows maintaining a constant read time while increasing the number of bitcells per column. The bitcell layout in Fig. 4 mostly limits the number

of multiplexed bit lines to be routed across the bitcell to 2 or 3 in 28nm bulk CMOS.

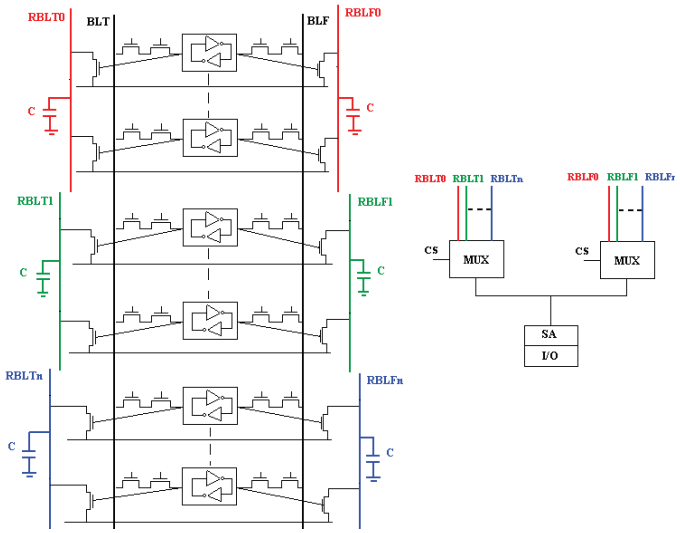

Figure 8. Proposed solution to increase the number of bitcells per column.

IV. COMPARISON WITH PREVIOUS BITCELLS

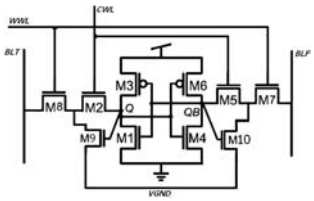

Figure 9. The 10T bitcell in [10]

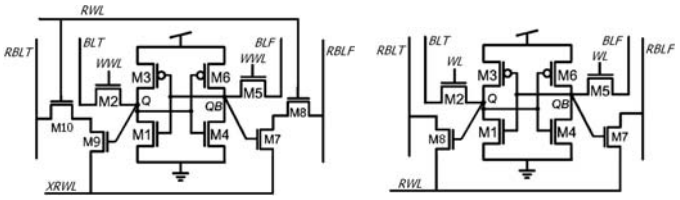

Figure 10. 10TVGND in [12] (left) and the zig-zag 8T in [13](right)

The design of the bitcell layout gains in flexibility when decoupling the write path from the read path: it offers acceptable performances under ULV whereas the 6T bitcell is obviously limited in SNM and WM. Recently in this context; 8T bitcells have been proposed [11] that feature a read-mode SNM equal to the hold-mode SNM. In the following, a comparative study concerns the SRAM bitcells ([10] [12] [13]) working under ULV in 32nm bulk CMOS.

All the results in this paper are obtained through SPICE simulations using a 32nm CMOS International Semiconductor Development Alliance (ISDA) model card. The sizing was performed and optimized in the same way for all bitcells.

The bitcells have been evaluated on the basis of SNM, WM, Write-Time (WT), Read current and Standby leakage current. All Monte Carlo simulations are performed with 1024 runs at 300 mV supply voltage and in worst-case temperature [-40°, 125°] and process corners. All criteria have been evaluated at three-sigma process variability.

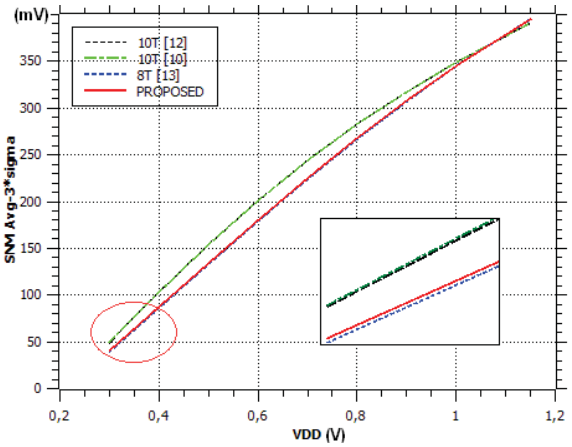

Figure 11. Comparison of the SNM for state-of-the-art ULV bitcells and the proposed 10T bitcell

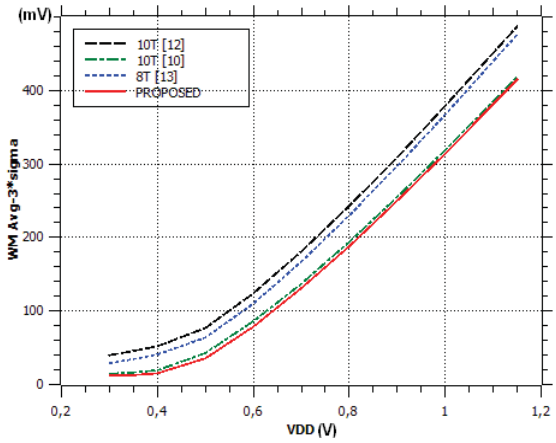

Figure 12. Comparison of the WM for state-of-the-art ULV bitcells and the proposed 10T bitcell

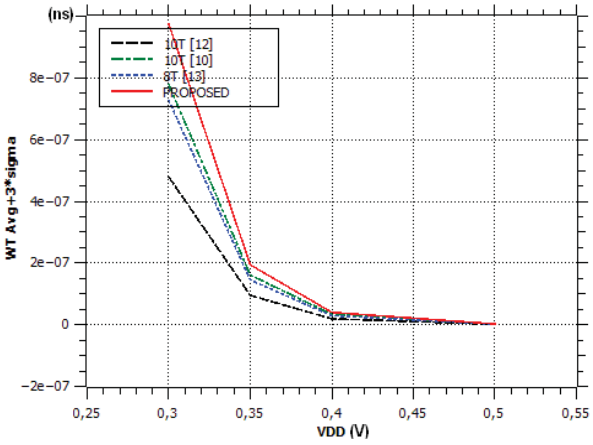

Figure 13. Comparison of the Write time for state-of-the-art ULV bitcells and the proposed 10T bitcell when VDD is scale

As shown in Fig 11 and Fig 12, the proposed bitcell has similar performance in terms of SNM and WM with respect to the other bitcells presented in this work. In Fig 13, we observe a small degradation in term of WT. This is due to the resistive path formed by the two series pass-gates transistors (M2 and M7) or (M2 and M8).

The analysis of leakage current in the different bitcells shows that there are two major sources of leakage: The current flowing from the bitline pre-charged to V_{DD} to the internal node equal to GND and the current through the read port.

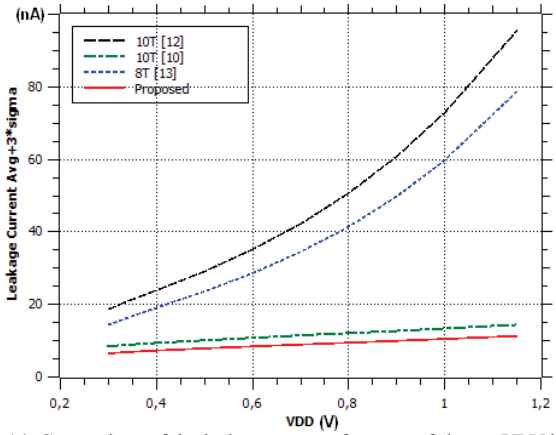

Figure 14. Comparison of the leakage current for state-of-the-art ULV bitcells and the proposed 10T bitcell

In the proposed bitcell both sources of leakage are weakened by the resistive path formed by the two series pass-gates transistors and the transistor in the read port which has source and drain at the same potential (RBL = RWL_MUX= V_{DD}). As shown in the Fig 14, the proposed bitcell is better in term of total leakage current. It is observed that the leakage current is almost constant as a function of the supply voltage. Hence the proposed bitcell is able to operate under ULV and also at the nominal voltage without a significant increase in leakage current. As shown in Fig 15 voltage scaling reduces as a square law the dynamic energy and linearly reduces the leakage power. Since delay increases exponentially, leakage energy increases and dominates total energy consumption at low VDD. In the TT process corner and at 25° C, the optimal voltage for the proposed bitcell is 350 mV.

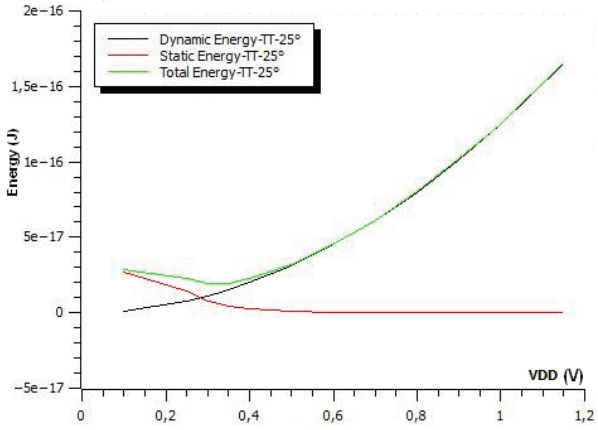

Figure 15. Active- and leakage-energy profiles of the proposed 10T

V. CONCLUSION:

This paper proposes a 10T bitcell which helps to alleviate main limitations of the state-of-the-art architectures (high leakage current and Dynamic parasitic power consumption) and which offers similar performances in terms of stability (SNM, WM) as the previously proposed ULV bitcells, at an inferior leakage current and at a superior read current (Table I). Dynamic parasitic power consumption is avoided in the half-select cells, thanks to a proposed hard coding technique. A comparative study was performed for ULV bitcells in 32nm CMOS. Simulations in worst-case corners yield pertinent trade-off architecture. Next step will be the silicon verification in 28nm CMOS.

TABLE I. PERFORMANCES OF VARIOUS BITCELLS IN 32 NM BULK CMOS UNDER ULV IN PT WORST-CASE

@ 300 mv Worst Case : T° & Process Corner	WT [µs] (Avg+3σ)	I_{LEAK} [nA] (Avg)	WM [mV] (Avg-3σ)	SNM [mV] (Avg-3σ)	I_{CELL} [nA] (Avg)
6T	failed	6.09	failed	failed	failed
10T [10]	0.79	5.54	14.7	**49.3**	1.83
10T [12]	**0.47**	10.3	**39.8**	39.7	1.41
8T [13]	0.53	7.42	28.8	39.4	5.46
Proposed	0.82	**4.13**	12.3	40.6	**5.52**

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